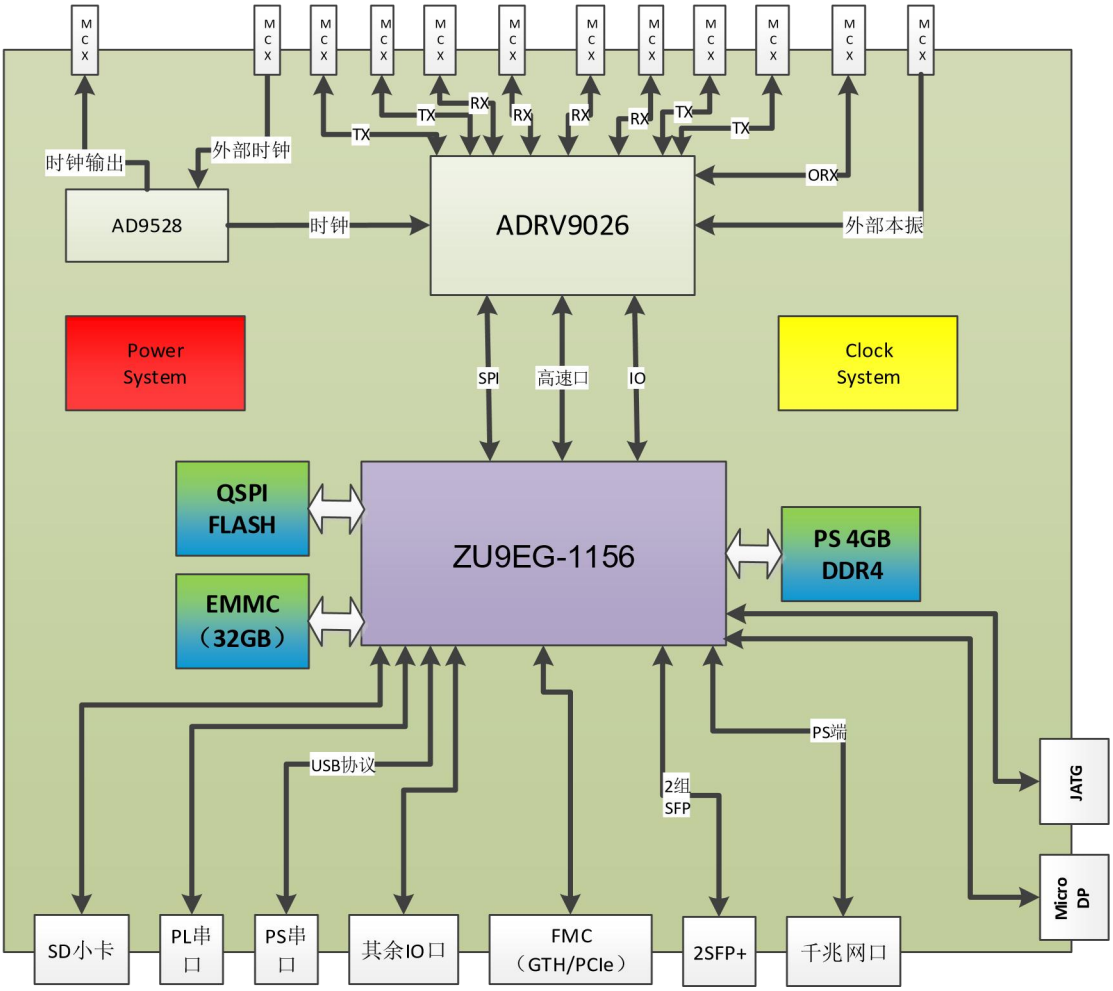
Quad Channel Embedded Software Defined Radio Platform

Product Brochure

Table of contents

1. Product Introduction

The four-channel embedded software radio platform is an embedded, miniaturized, low-power software radio platform developed for various wireless communication product development and communication teaching. The platform is composed of two parts, one is a radio frequency signal transceiver module developed based on ADI's ADRV9026 chip, and the other is a back-end digital processing module based on Xilinx's Zynq UltraScale+ chip XCZU15EG-FFVB1156. This platform is a high-performance, highly integrated wireless radio frequency signal transceiver processing equipment, suitable for the development of wireless ad hoc network nodes, wireless communication teaching aids, miniaturized spectrum detection, mini signal generators, wireless point direction finding and positioning development, etc. .


MCX
时钟输出
外部时钟
AD9528
时钟
ADRV9026
外部本振
TX
RX
ORX
Power System
Clock System
SPI
高速口
IO
QSPI FLASH
EMMC（32GB）
ZU9EG-1156
PS 4GB DDR4
USB协议
PS端
2组SFP
JATG
Micro DP
SD小卡
PL串口
PS串口
其余IO口
FMC（GTH/PCIe）
2SFP+
千兆网口

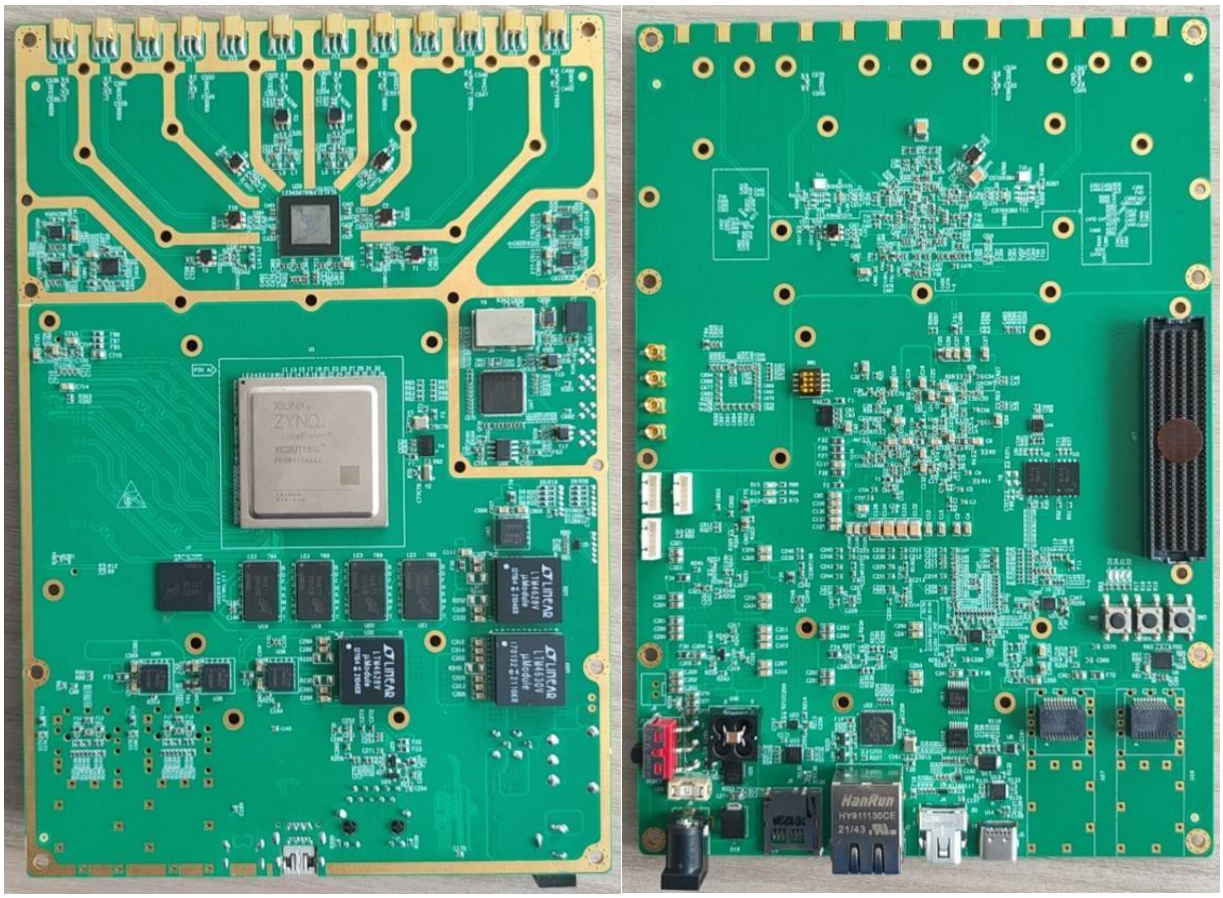


Figure 1-1 Front and back of the board

The basic performance indicators of the platform are as follows:

- Baseband processor: XCZU15EG-FFVB1156
- RF chip: ADRV9026
- Interface: Ethernet port, serial port, PL/PS I/O port, JTAG port, dual 10GSFP+, TF card, micro DP
- Onboard FLASH, can be configured to start by FLASH or TF card through the DIP switch

- Onboard 4GB DDR4 (PS side)
- Onboard 32GB EMMC memory, coping with high vibration environment
- Size: 200mm×140mm
- The onboard 9528 clock chip reserves two clock outputs and two reference clock inputs, which can be used for inter-board cascaded clock synchronization
- Onboard FMC HPC interface, the interface definition follows the VITA standard protocol, which can be extended to PCIe interface, NVMe SSD interface, multi-channel optical port or used for high-speed data communication between multiple boards.

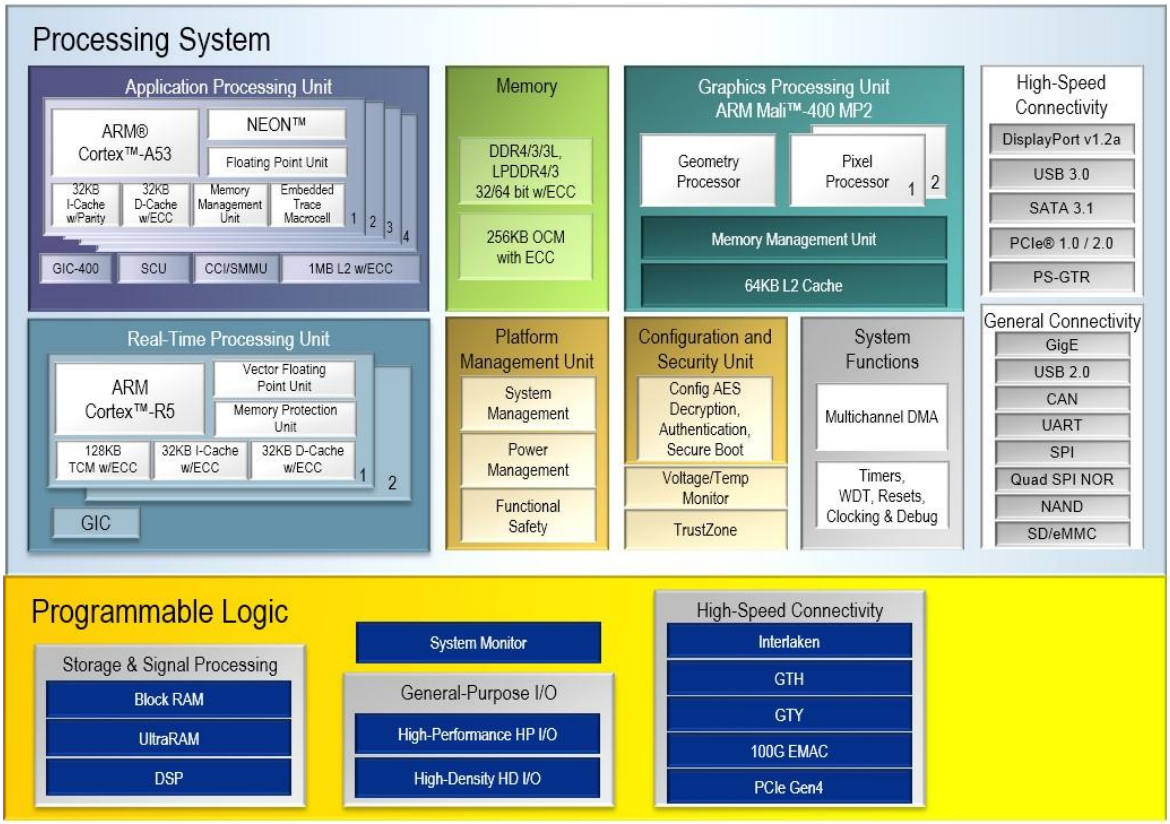
1.1 XCZU15EG-FFVB1156 chip introduction

The board uses the Zynq UltraScale+ series chip of Xilinx Company, the model is XCZU15EG-FFVB1156. The chip's PS system integrates a quad-core ARM Cortex-A53 processor as an application processing unit, and a dual-core ARM Arm Cortex-R5F processor as a real-time processing unit. On-chip integrates AMBA® interconnect, internal memory, external memory interface and peripherals. These peripherals mainly include USB bus interface, Ethernet interface, SD/SDIO interface, I2C bus interface, CAN bus interface, UART interface, GPIO and so on. The PS can run independently and start on power-up or reset.

Basic parameters of baseband processor:

- Application Processing Unit: Quad-core Arm® Cortex®-A53 MPCore™ up to 1.5GHz

- Real-time processing unit: Dual-core Arm Cortex-R5F MPCore™ (up to 600MHz)
- Graphics Processing Unit: Arm Mali™-400 MP2 up to 667MHz
- FPGA logic unit: 747k
- Memory: 57.7Mb
- DSP slices: 3528



1.2 ADRV9026 chip introduction

ADI's 4th Generation Wideband RF Transceiver ADRV9026 Offers Four-Channel Integration with Lowest Power, Smallest

Size Common Platform Solution Simplifies Design of 3G/4G/5G Applications Including Multistandard Base Stations, Massive MIMO and Small Cells And reduce its system power consumption, size, weight and cost.

Basic parameters of RF front-end

- RF channel: 4 transmissions and 4 receptions, 2 observation and reception ORX channels
- Clock: 9528 clock synchronization chip, reserved two external local oscillator interfaces
- RF working range: 75MHz to 6GHz,
- Bandwidth: maximum receive bandwidth 200MHz, maximum transmit bandwidth 200MHz
- Sampling rate: up to 245.76MSPS

1.3 product

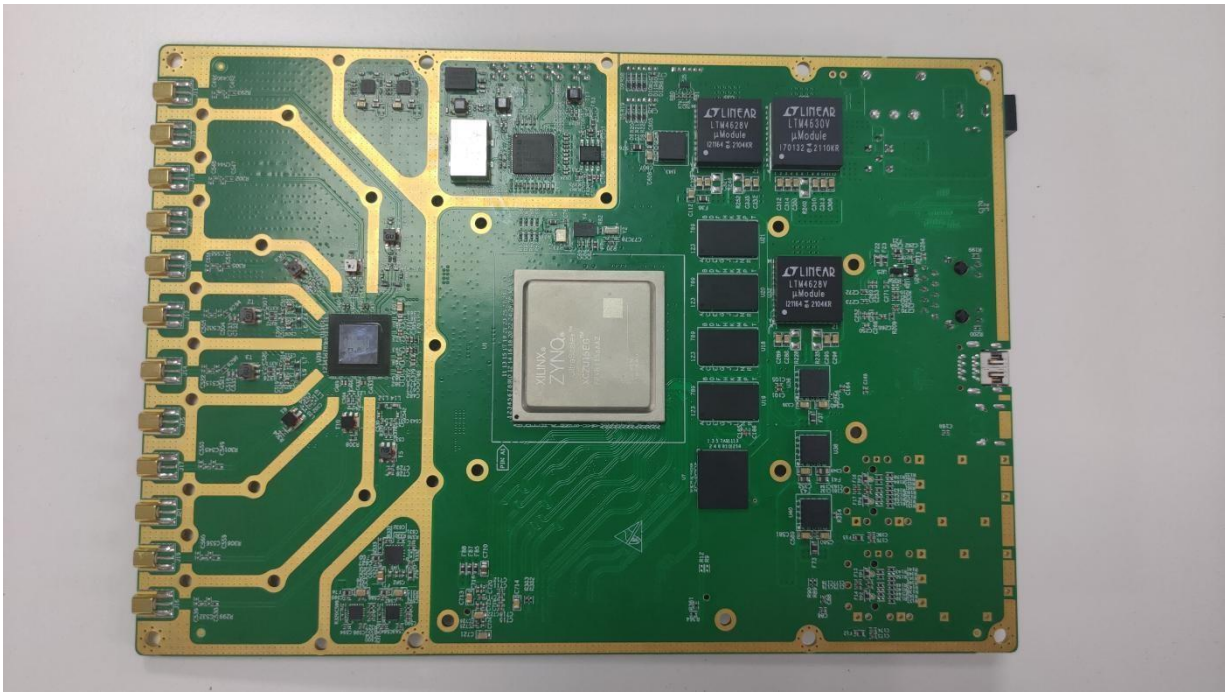


Figure 1-2 Front view of the board

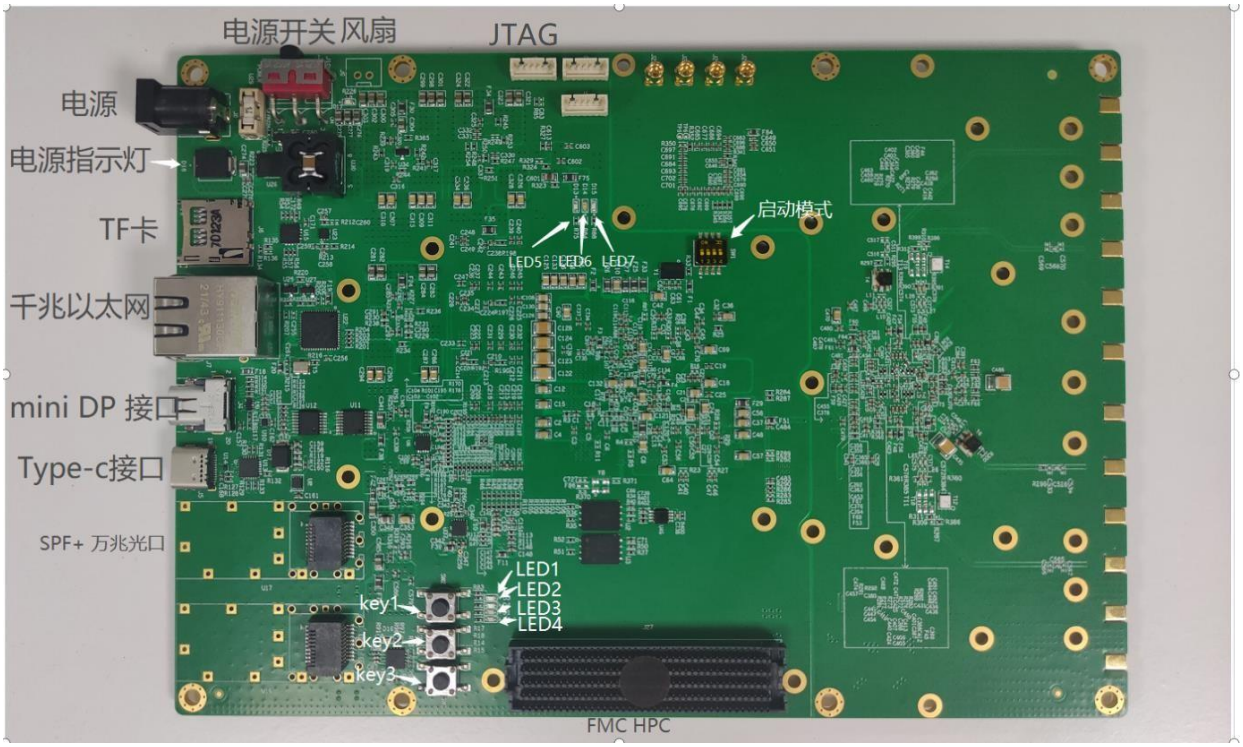


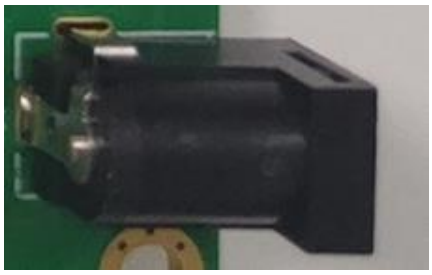
Figure 1-3 Interface definition on the back of the board

2 Interface Description

2.1 Main power interface

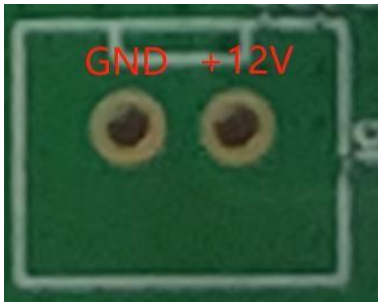
The main power supply is powered by +12V, and the maximum allowable input voltage is 14V. It is recommended to use a 12V5A power supply for power supply. The interface type of the main power supply is DC round hole 5.5-2.5.

Note: The fan and FMC 12V power supply are connected in parallel with the main power supply, excessive voltage may burn the fan and FMC equipment.



2.2 fan interface

board outputs a +12V power supply (connected in parallel with the power supply, and the specific voltage is consistent with the power supply voltage), which can supply power for the fan. When the board is used, please install a fan for good heat dissipation, otherwise there is a risk of burning.

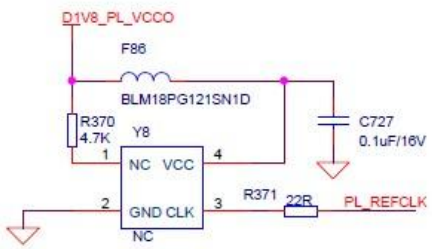


2.3 clock

2.3.1 PL clock

onboard 200MHz clock chip provides the clock for the PL terminal.

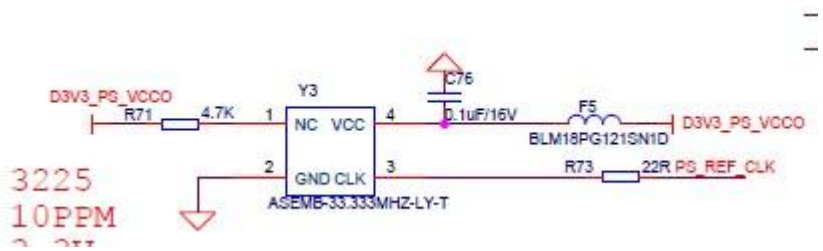
Note: The current PL clock is not welded, please explain in advance if necessary.



name	Pin name
PL_REFCLK	IO_L12P_T1U_N10_GC_66

2.3.2 ps clock

onboard 33.333333MHz clock chip provides the clock for the PS side.



name	Pin name
PS_REF_CLK	PS_REF_CLK
PS_PADI	PS_PADI
PS_PADO	PS_PADO

2.3.3 Optical port clock

onboard 156.25MHz clock chip provides the clock for the optical port.

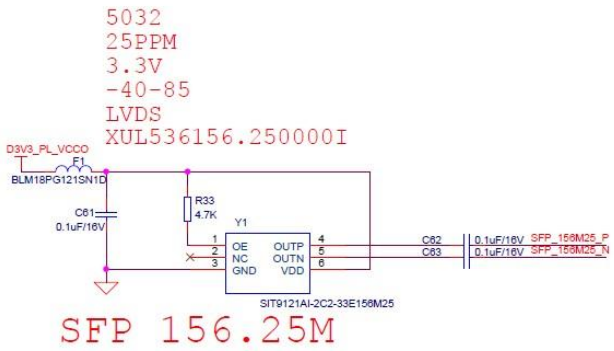


Figure 2-5 Optical port clock

Table 2-3 Optical port clock pin correspondence

name	pin name
SFP_156M25_P	MGTREFCLK1P_128
SFP_156M25_N	MGTREFCLK1N_128

2.4 Gigabit Ethernet

The board has a standard RJ45 Gigabit Ethernet interface, which is connected to the PS end. The PHY chip model is 88E1512, and the RJ45 interface is HY911130CE. The port has a network transformer to ensure the network connectivity between different network devices.

Table 2-4 Correspondence of Ethernet port pins

name	Pin name
ETH1_TXCK	PS_MIO64
ETH1_TXD0	PS_MIO65
ETH1_TXD1	PS_MIO66
ETH1_TXD2	PS_MIO67
ETH1_TXD3	PS_MIO68
ETH1_TXCTL	PS_MIO69
ETH1_RXCK	PS_MIO70
ETH1_RXD0	PS_MIO71
ETH1_RXD1	PS_MIO72
ETH1_RXD2	PS_MIO73
ETH1_RXD3	PS_MIO74
ETH1_RXCTL	PS_MIO75
ETH1_MDC	PS_MIO76

ETH1_MDIO	PS_MIO77

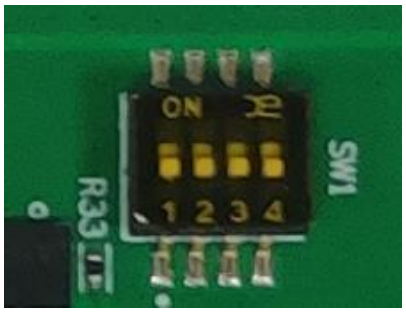
2.5 TF card

There is a TF card interface on the board, which is connected to the PS side. The corresponding relationship between the pins is as follows Table 2-5 Correspondence of TF pins

name	Corresponding pin name
MIO45_SDIO_DETECT	PS_MIO45
MIO46_SDIO_DAT0	PS_MIO46
MIO46_SDIO_DAT1	PS_MIO47
MIO46_SDIO_DAT2	PS_MIO48
MIO46_SDIO_DAT3	PS_MIO49
MIO46_SDIO_CMD	PS_MIO50
MIO46_SDIO_CLK	PS_MIO51

2.6 boot mode

The board uses a 4-bit DIP switch to switch the startup mode of the board.



2-6 DIP switch up to 0, down to 1.

Table 2-6 Start mode selection table

	Key1	Key2	Key3	Key4
PS JTAG	0	0	0	0
Quad-SPI(24b)	0	0	0	1
Quad-SPI(32b)	0	0	1	0
SD0(2.0)	0	0	1	1
NAND	0	1	0	0
SD1(2.0)	0	1	0	1
eMMC(1.8V)	0	1	1	0
USB0(2.0)	0	1	1	1
PJTAG(MIO #0)	1	0	0	0
PJTAG(MIO #1)	1	0	0	1
SD1 LS（3.0）	1	1	1	0

2.7 The miniDP interface

board has a miniDP interface, which is connected to the PS side. The model of the DP interface is MINI DP_2129320-3.

Table 2-7 DP interface pin correspondence

name	Pin name	pin number
DP_TX1_P	PS_MGTRTXP1_505	Y29

DP_TX1_N	PS_MGTRTXN1_505	Y30
DP_TX0_P	PS_MGTRTXP0_505	AB29
DP_TX0_N	PS_MGTRTXN0_505	AB30
MIO27_DP_AUX_OUT	PS_MIO27	M21
MIO29_DP_OE	PS_MIO29	K22
MIO30_DP_AUX_IN	PS_MIO30	L21
MIO28_DP_HPD	PS_MIO28	N21

2.8 SFP+ Interface

There are two SFP interfaces on board, and the pin names of the high-speed optical interface connections are shown in the table below.

Table 2-8 Correspondence of SPF interface pins

name	Pin name	pin number
SFP1_TX_P	MGTHTXP0_128	T29
SFP1_TX_N	MGTHTXN0_128	T30
SFP2_TX_P	MGHT XP1_128	R31
SFP2_TX_N	MGTHTXN1_128	R32
SFP1_RX_P	MGTHRXP0_128	T33
SFP1_RX_N	MGTHRXN0_128	T34

SFP2_RX_P	MGTHRXP1_128	P33
SFP2_RX_N	MGTHRXN1_128	P34
SFP1_CLK_N	MGTREFCLK0N_128	R28
SFP1_CLK_P	MGTREFCLK0P_128	R27

2.9 FMC HPC

Table 2-9 FMC HPC interface pin correspondence

name	Pin name	name	Pin name
FMC1_DP1_M2C_P	MGTHRXP0_228	FMC1_DP9_M2C_P	MGTHRXP0_229
FMC1_DP1_M2C_N	MGTHRXN0_228	FMC1_DP9_M2C_N	MGTHRXN0_229
FMC1_DP2_M2C_P	MGTHRXP2_228	FMC1_DP8_M2C_P	MGTHRXP1_229

FMC1_DP2_M2C_N	MGTHRXN2_228	FMC1_DP8_M2C_N	MGTHRXN1_229
FMC1_DP3_M2C_P	MGTHRXP3_228	FMC1_DP7_M2C_P	MGTHRXP0_230
FMC1_DP3_M2C_N	MGTHRXN3_228	FMC1_DP7_M2C_N	MGTHRXN0_230
FMC1_DP4_M2C_P	MGTHRXP1_230	FMC1_DP6_M2C_P	MGTHRXP2_230
FMC1_DP4_M2C_N	MGTHRXN1_230	FMC1_DP6_M2C_N	MGTHRXN2_230
FMC1_DP5_M2C_P	MGTHRXP3_230	FMC1_GBTCLK1_M2C_P	MGTREFCLK0P_230
FMC1_DP5_M2C_N	MGTHRXN3_230	FMC1_GBTCLK1_M2C_N	MGTREFCLK0N_230
FMC1_DP1_C2M_P	MGTHTXP0_228	FMC1_DP9_C2M_P	MGTHTXP0_229
FMC1_DP1_C2M_N	MGTHTXN0_228	FMC1_DP9_C2M_N	MGTHTXN0_229
FMC1_DP2_C2M_P	MGTHTXP2_228	FMC1_DP8_C2M_P	MGTHTXP1_229
FMC1_DP2_C2M_N	MGTHTXN2_228	FMC1_DP8_C2M_N	MGTHTXN1_229
FMC1_DP3_C2M_P	MGTHTXP3_228	FMC1_DP7_C2M_P	MGTHTXP0_230
FMC1_DP3_C2M_N	MGTHTXN3_228	FMC1_DP7_C2M_N	MGTHTXN0_230
FMC1_DP4_C2M_P	MGTHTXP1_230	FMC1_DP6_C2M_P	MGTHTXP2_230
FMC1_DP4_C2M_N	MGTHTXN1_230	FMC1_DP6_C2M_N	MGTHTXN2_230
FMC1_DP5_C2M_P	MGTHTXP3_230		
FMC1_DP5_C2M_N	MGTHTXN3_230		
FMC1_DP0_C2M_P	MGTHTXP1_228	VADJ_FMC_PGOOD	PGOOD1
FMC1_DP0_C2M_N	MGTHTXN1_228	FMC1_GBTCLK0_M2C_P	MGTREFCLK1N_228
FMC1_DP0_M2C_P	MGTHRXP1_228	FMC1_GBTCLK0_M2C_N	MGTREFCLK1P_228
FMC1_DP0_M2C_N	MGTHRXN1_228	FMC1_LA01_P_HP_ CC	IO_L7P_T1L_N0_QBC_AD13P_64
FMC1_LA06_P_HP	IO_L7N_T1L_N1_QBC_AD13N_65	FMC1_LA01_N_HP_CC	IO_L7N_T1L_N1_QBC_AD1 3N_64
FMC1_LA06_N_HP	IO_L7P_T1L_N0_QBC_AD13 P_65	FMC1_LA05_P_HP	IO_L11P_T1U_N8_GC_65
FMC1_LA10_P_HP	IO_L5N_T0U_N9_AD14N_65	FMC1_LA05_N_HP	IO_L11N_T1U_N9_GC_65
FMC1_LA10_N_HP	IO_L5P_T0U_N8_AD14P_65	FMC1_LA09_P_HP	IO_L8P_T1L_N2_AD5P_64
FMC1_LA14_P_HP	IO_L6N_T0U_N11_AD6N_65	FMC1_LA09_N_HP	IO_L8N_T1L_N3_AD5N_64

FMC1_LA14_N_HP	IO_L6P_T0U_N10 _AD6P_65	FMC1_LA13_P_HP	IO_L24P_T3U_N10_6 4
FMC1_LA18_P_HP_ CC	IO_L16N_T2U_N7 _QBC_AD3 N_64	FMC1_LA13_N_HP	IO_L24N_T3U_N11_ 64
FMC1_LA18_N_HP_ CC	IO_L16P_T2U_N6 _QBC_AD3 P_64	FMC1_LA17_P_HP_ CC	IO_L10P_T1U_N6_Q BC_AD 4P_64
FMC1_LA27_P_HP	IO_L15N_T2L_N5 _AD11N_64	FMC1_LA17_N_HP_ CC	IO_L10N_T1U_N7_Q BC_A D4N_64
FMC1_LA27_N_HP	IO_L15P_T2L_N4 _AD11P_64	FMC1_LA23_P_HP	IO_L17P_T2U_N8_A D10P_6 5
		FMC1_LA23_N_HP	IO_L17N_T2U_N9_A D10N_ 65
		FMC1_LA26_P_HP	IO_L9P_T1L_N4_AD 12P_65
		FMC1_LA26_N_HP	IO_L9N_T1L_N5_AD 12N_6 5
FMC1_CLK1_M2C_P _HP	IO_L12N_T1U_N1 1_GC_64	FMC1_CLK0_M2C_ P_HP	IO_L14P_T2L_N2_G C_64
FMC1_CLK1_M2C_ N_HP	IO_L12P_T1U_N1 0_GC_64	FMC1_CLK0_M2C_ N_HP	IO_L14N_T2L_N3_ GC_64
FMC1_LA00_P_HP_	IO_L13P_T2L_N0 _GC_QBC_	FMC1_LA02_P_HP	IO_L18P_T2U_N10_A D2P_6 4
CC	64		
FMC1_LA00_N_HP_ CC	IO_L13N_T2L_N1 _GC_QBC_ 64	FMC1_LA02_N_HP	IO_L18N_T2U_N11_ AD2N_ 64
FMC1_LA03_P_HP	IO_L6P_T0U_N10 _AD6P_64	FMC1_LA04_P_HP	IO_L15P_T2L_N4_A D11P_6 5
FMC1_LA03_N_HP	O_L6N_T0U_N11 _AD6N_64	FMC1_LA04_N_HP	IO_L15N_T2L_N5_A D11N_ 65
FMC1_LA08_P_HP	IO_L13P_T2L_N0_ GC_QBC_ 65	FMC1_LA07_P_HP	IO_L9P_T1L_N4_AD 12P_64
FMC1_LA08_N_HP	IO_L13N_T2L_N1 _GC_QBC_ 65	FMC1_LA07_N_HP	IO_L9N_T1L_N5_A D12N_6 4
FMC1_LA12_P_HP	IO_L17P_T2U_N8 _AD10P_64	FMC1_LA11_P_HP	IO_L22P_T3U_N6_D BC_AD 0P_64
FMC1_LA12_N_HP	IO_L17N_T2U_N9	FMC1_LA11_N_HP	IO_L22N_T3U_N7_D

	_AD10N_6 4		BC_A D0N_64
FMC1_LA16_P_HP	IO_L16P_T2U_N6 _QBC_AD3 P_65	FMC1_LA15_P_HP	IO_L19P_T3L_N0_D BC_AD 9P_65
FMC1_LA16_N_HP	IO_L16N_T2U_N7 _QBC_AD3 N_65	FMC1_LA15_N_HP	IO_L19N_T3L_N1_D BC_AD 9N_65
FMC1_LA20_P_HP	IO_L20P_T3L_N2 _AD1P_65	FMC1_LA19_P_HP	IO_L8P_T1L_N2_AD 5P_65
FMC1_LA20_N_HP	IO_L20N_T3L_N3 _AD1N_65	FMC1_LA19_N_HP	IO_L8N_T1L_N3_AD 5N_65
FMC1_LA22_P_HP	IO_L18P_T2U_N1 0_AD2P_65	FMC1_LA21_P_HP	IO_L12P_T1U_N10_ GC_65
FMC1_LA22_N_HP	IO_L18N_T2U_N1 1_AD2N_65	FMC1_LA21_N_HP	IO_L12N_T1U_N11_ GC_65
FMC1_LA25_P_HP	IO_L20P_T3L_N2 _AD1P_64	FMC1_LA24_P_HP	IO_L19P_T3L_N0_D BC_AD 9P_64
FMC1_LA25_N_HP	IO_L20N_T3L_N3 _AD1N_64	FMC1_LA24_N_HP	IO_L19N_T3L_N1_D BC_AD 9N_64
FMC1_LA29_P_HP	IO_L21P_T3L_N4 _AD8P_64	FMC1_LA28_P_HP	IO_L23P_T3U_N8_6 4
FMC1_LA29_N_HP	IO_L21N_T3L_N5 _AD8N_64	FMC1_LA28_N_HP	IO_L23N_T3U_N9_6 4
FMC1_LA31_P_HP	IO_L22P_T3U_N6 _DBC_AD0 P_65	FMC1_LA30_P_HP	IO_L21P_T3L_N4_A D8P_65
FMC1_LA31_N_HP	IO_L22N_T3U_N7 _DBC_AD0 N_65	FMC1_LA30_N_HP	IO_L21N_T3L_N5_A D8N_6 5
FMC1_LA33_P_HP	IO_L24N_T3U_N1 1_PERSTN 0_65	FMC1_LA32_P_HP	IO_L23P_T3U_N8_I2 C_SCL K_65
FMC1_LA33_N_HP	IO_L24P_T3U_N10 _PERSTN1_I2C_S DA_65	FMC1_LA32_N_HP	IO_L23N_T3U_N9_6 5

2.10 Type-c to internal PS PL serial port

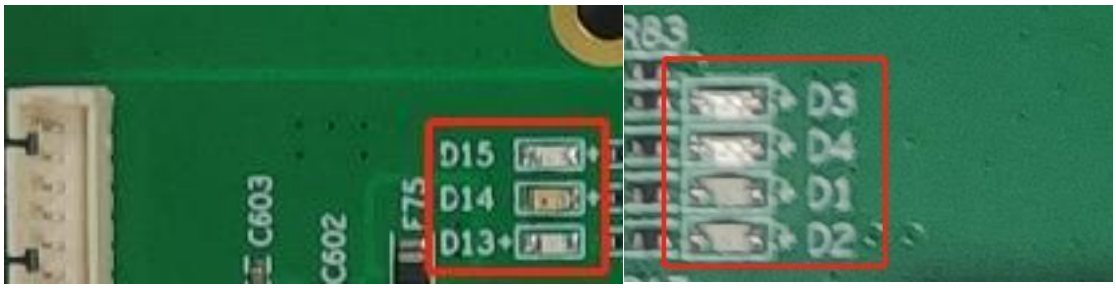
PS connects to the PL end to each lead to a serial port, which is converted to a USB Type-C interface by the CP2105 chip .

Table 2-10 Type-c interface pin correspondence table

name	Pin name
UART_MIO34_RXD	PS_MIO34
UART_MIO35_TXD	PS_MIO35
UART_PL_TXD	IO_L7N_HDGC_49
UART_PL_RXD	IO_L7P_HDGC_49

2.11 led

7 LEDs on the board , as shown in the figure below, there are 3 LEDs on the upper left of the dial switch on the back (interface surface) of the board , from left to right they are LED (D13), LED (D14), LED (D15). Board back (Interface surface) There are four LEDs next to the button, which are LED (D3), LED (D4), LED (D1), and LED (D2) from top to bottom .



LED label	Connection pin name	Connection pin number
D1	IO_L2N_AD10N_44	AN13
D2	IO_L3N_AD9N_44	AP12
D3	IO_L1N_AD11N_44	AP14
D4	IO_L1P_AD11P_44	AN14
D13	PS_DONE	W21
D14	PS_ERR_OUT	T21
D15	PS_ERR_STATUS	R21

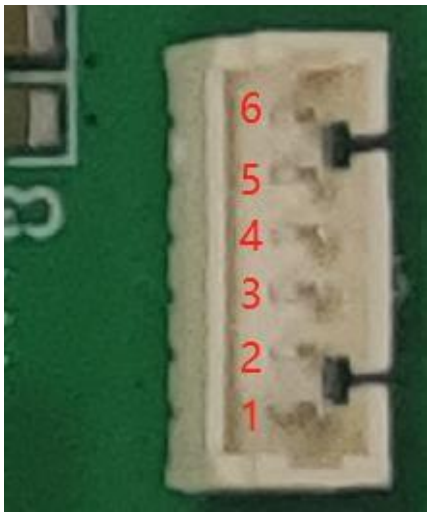
2.12 DDR4

The board is mounted with four 1GB DDR4 chips to form 4G DDR4, the bit width is 64 bits, and the model of the four chips is

MT40A512M16JY-083E is composed of chips, which are mounted on the MIO BANK504 on the PS side .

2.13 JTAG

Use 6-pin 1.25mm pitch terminals. The silkscreen on the board is J3.



Line order	name	Pin name	pin number
1	VCC_3.3V	VCC_3.3V	Internally connected to 3.3V power supply
2	GND	GND	GND
3	FPGA_JTAG_TMS	PS_JTAG_TMS	R24
4	FPGA_JTAG_TCK	PS_JTAG_TCK	R25
5	FPGA_JTAG_TDO	PS_JTAG_TDO	T25
6	FPGA_JTAG_TDI	PS_JTAG_TDI	U25

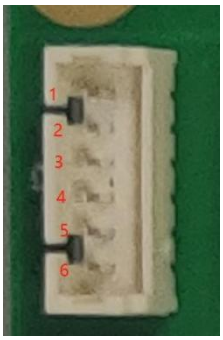
2.14 IO

PL end leads to 4 IOs, the pin level is 3.3V, and the label is J1

Line order	name	Pin name	pin number
1	PL_GPIO 1	IO_L11P_AD1P_47	A21
2	PL_GPIO 2	IO_L7N_HDGC_AD5N_ 47	D22
3	PL_GPIO 3	IO_L11N_AD1N_47	A22
4	PL_GPIO 4	IO_L9N_AD3N_47	C22
5	VCC_3.3 V	VCC_3.3V	Internall y connected to 3.3V power

			supply
6	GND	GND	GND

PS end leads to 4 IOs , and the IO level is 1.8V , labeled J2 .



Line order	name	Pin name	pin number
1	PS_GPIO1	PS_MIO52	F22
2	PS_GPIO2	PS_MIO53	E23
3	PS_GPIO3	PS_MIO54	F23
4	PS_GPIO4	PS_MIO55	B23
5	VCC_1.8V	VCC_1.8V	Internally connected to 1.8V power supply
6	GND	GND	GND

2.15 There are three buttons on the button board, which are located next to the FMC HPC, and their labels are SW2, SW3, and SW4 respectively.

Figure 2-11 Board buttons

Table 2-15 Board button pin correspondence

name	Pin name	pin number
SW2	PS_PROG_B	U21
SW3	PS_POR_B	V23
SW4	PS_SRST_B	U23

2.16 FLASH

onboard 64MB QSPI FLASH is composed of dual S25FS256SAGNFI001 chips, and its pins correspond to shown in the table below.

Table 2-16 QSPIFLASH pins

name	Corresponding pin name
MIO0_QSPI_LWR_CLK	PS_MIO0
MIO1_QSPI_LWR_DQ1	PS_MIO1
MIO2_QSPI_LWR_DQ2	PS_MIO2
MIO3_QSPI_LWR_DQ3	PS_MIO3
MIO4_QSPI_LWR_DQ0	PS_MIO4
MIO5_QSPI_LWR_CS_B	PS_MIO5
MIO7_QSPI_UPR_CS_B	PS_MIO7
MIO8_QSPI_UPR_DQ0	PS_MIO8
MIO9_QSPI_UPR_DQ1	PS_MIO9
MIO10_QSPI_UPR_DQ2	PS_MIO10

2.17 AD9528

AD9528 on board is used for clock synchronization.

AD9528 has two off-board clock input and clock output, as shown in the figure below, see below for details.

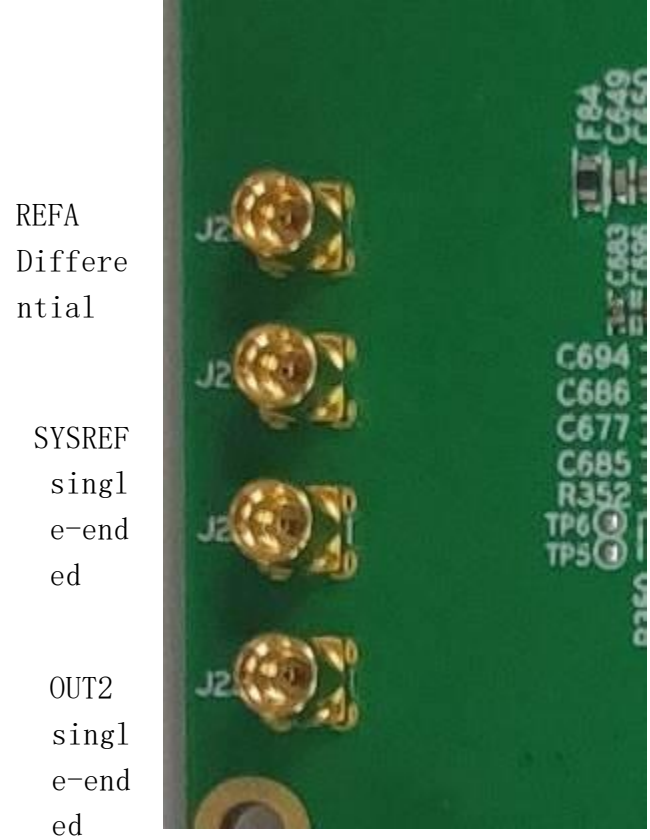


Figure 2-12 AD9528 two-way off-board clock input and clock output

2.17.1 clock input

AD9528 clock is onboard 122.88MHz clock crystal oscillator, which is connected to pin 8 of AD9528 through a matching network .

The AD9528 REFB signal is provided by the onboard 30.72MHz differential clock, the REFA signal is connected to the J23

interface through the balun, and the SYSREF signal is drawn to the J24 interface. The interface form is MMCX.

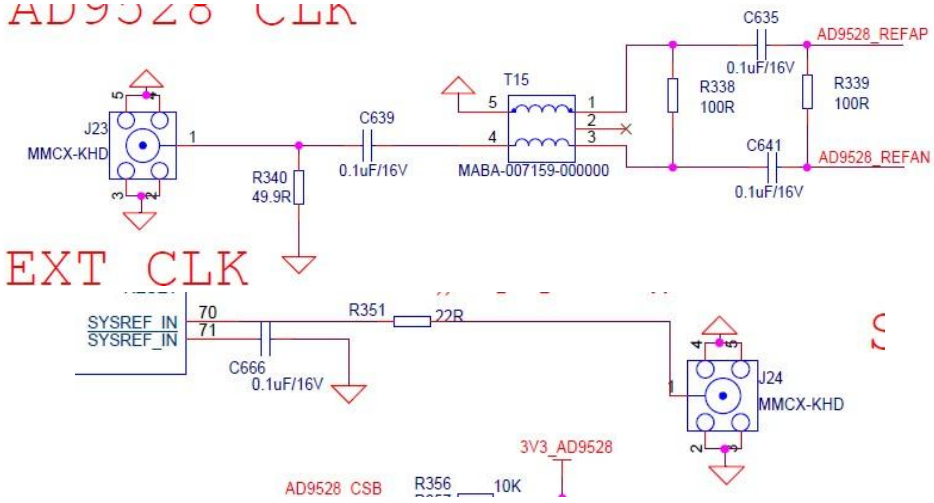


Figure 2-13 AD9528 clock input

2.17.2 control signal

Note: FPGA_SYSREF_REQ can be switched to FPGA or ground through two resistors R350 and R352.

Connect to FPGA when R350 is soldered, and connect to ground when R352 is soldered. Connected to ground by default

Table 2-17 AD9528 control signals

name	AD9528 pin number	pin number
FPGA_9528_SDO	twenty four	B19

FPGA_9528_SDI	twenty three	A18
FPGA_9528_SDCLK	twenty two	B18
FPGA_9528_CSB	twenty one	C18
FPGA_9528_RESETB	19	A17
FPGA_SYSREF_REQ	57	C19

2.17.3 clock output

AD9528 outputs two clocks to the outside of the board, the positive signal of OUT2 is directly led to J26, the differential of OUT3 is led to J25 through the balun , and the interface form is MMCX.

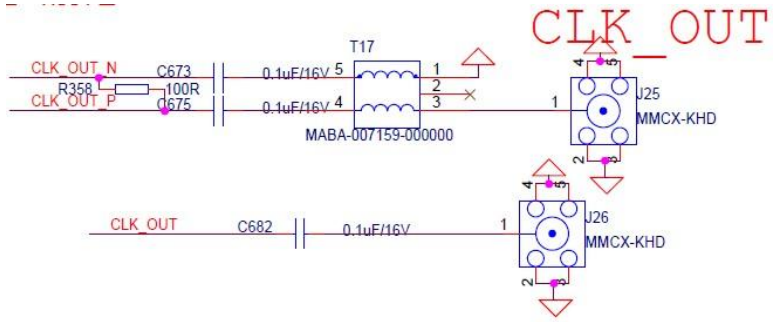


Figure 2-14 AD9528 clock output Table 2-18 AD9528 clock output

name	AD9528 pin number	connected to	Corresponding pin number
OUT0_N	68	SERDES_CLK_N_2	B9
OUT0_P	67	SERDES_CLK_P_2	B10

OUT1_N	65	SERDES_CLK_N_3	E7
OUT1_P	64	SERDES_CLK_P_3	E8
OUT2_P	61	J26	1
OUT3_N	59	J25	1
OUT3_P	58	J25	1
OUT4_N	53	SERDES_CLK_N_1	L7
OUT4_P	52	SERDES_CLK_P_1	L8
OUT5_N	50	SYSREF_N_FPGA	Y3
OUT5_P	49	SYSREF_P_FPGA	Y4
OUT6_N	47	9026_JESD204B_CLK_N	L28
OUT6_P	46	9026_JESD204B_CLK_P	L27
OUT7_N	44	SFP1_CLK_N	R28
OUT7_P	43	SFP1_CLK_P	R27
OUT9_N	38	REFCLK_N_FPGA	AA5
OUT9_P	37	REFCLK_P_FPGA	Y5
OUT10_N	35	REFCLK_N1_FPGA	AG4
OUT10_P	34	REFCLK_P1_FPGA	AG5
OUT11_N	32	REFCLK_N2_FPGA	F20
OUT11_P	31	REFCLK_P2_FPGA	G20

OUT12_N	29	9026_DEV_CLK_IN-	C9
OUT12_P	28	9026_DEV_CLK_IN+	C8
OUT13_N	26	9026_SYSREF_IN-	D9
OUT13_P	25	9026_SYSREF_IN+	D8

2.18 ADRV9026

adrv9026 has 12 interfaces including 4 RF inputs, 4 RF outputs, 2 external clocks, and 2 observation inputs . The interface is MMCX, as shown in the figure below

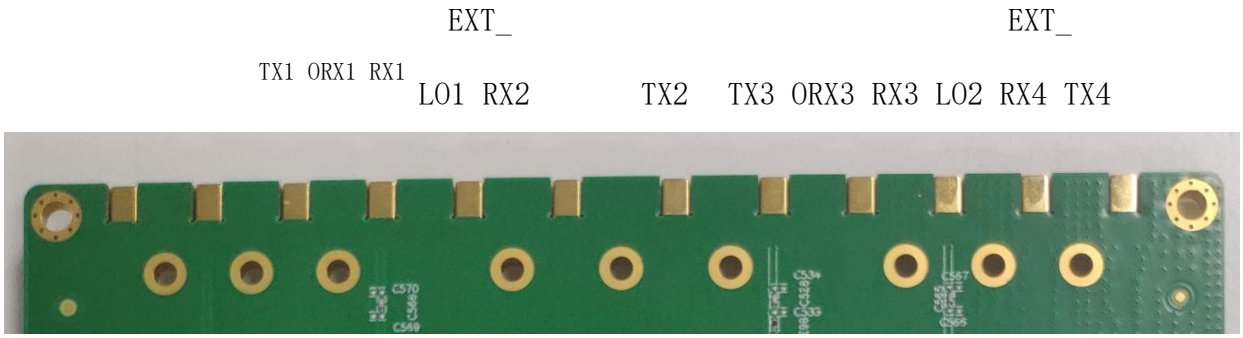


Figure 2-15 ADRV9026 output interface table 2-19 9026 interface pin correspondence table

name	Corresponding pin name	name	Corresponding pin name
9026_SERDINC+	MGHT XP2_129	9026_GPIO0	IO_L19P_T3L_N0_DBC_AD9P_67
9026_SERDINC-	MGTHTXN2_129	9026_GPIO1	IO_L20P_T3L_N2_AD1P_67

9026_SERDINA+	MGTHTXP0_129	9026_GPIO2	IO_L17N_T2U_N9_AD10N_66
9026_SERDINA-	MGTHTXN0_129	9026_GPIO3	IO_L24N_T3U_N11_66
9026_SERDINB+	MGHT XP1_129	9026_GPIO4	IO_L23N_T3U_N9_66
9026_SERDINB-	MGTHTXN1_129	9026_GPIO5	IO_L22N_T3U_N7_DBC_AD0N_67
9026_SERDIND+	MGTHTXP3_129	9026_GPIO6	IO_L24P_T3U_N10_67
9026_SERDIND-	MGTHTXN3_129	9026_GPIO7	IO_L5P_T0U_N8_AD14P_67
9026_SYNCINB1+	IO_L2P_T0L_N2_66	9026_GPIO8	IO_L23P_T3U_N8_67
9026_SYNCINB1-	IO_L2N_T0L_N3_66	9026_GPIO9	IO_L17P_T2U_N8_AD10P_67
9026_SYNCINB2	IO_L4P_T0U_N6_DBC_ AD7P_66	9026_GPIO10	IO_L14N_T2L_N3_GC_67

+			
9026_SYNCINB2 -	IO_L4N_T0U_N7_DBC_ AD7N_66	9026_GPIO11	IO_L17N_T2U_N9_AD10N_67
9026_SYNCINB3 +	IO_L1P_T0L_N0_DBC_6 6	9026_GPIO12	IO_L14P_T2L_N2_GC_67
9026_SYNCINB3 -	IO_L1N_T0L_N1_DBC_6 6	9026_GPIO13	IO_L12N_T1U_N11_GC_67
9026_SERDOUT A+	MGTHRXP0_129	9026_GPIO14	IO_L12P_T1U_N10_GC_67
9026_SERDOUT A-	MGTHRXN0_129	9026_GPIO15	IO_L21P_T3L_N4_AD8P_66
9026_SERDOUT C+	MGTHRXP2_129	9026_GPIO16	IO_L24P_T3U_N10_66
9026_SERDOUT C-	MGTHRXN2_129	9026_GPIO17	IO_L16N_T2U_N7_QBC_AD3N_67

9026_SERDOUT B+	MGTHRXP1_129	9026_GPIO18	IO_T3U_N12_66
9026_SERDOUT B-	MGTHRXN1_129	9026_CSB	IO_L18N_T2U_N11_AD2N_67
9026_SERDOUT D+	MGTHRXP3_129	9026_SDIO	IO_L21N_T3L_N5_AD8N_66
9026_SERDOUT D-	MGTHRXN3_129	9026_SDO	IO_L22N_T3U_N7_DBC_AD0N_66
9026_SYNCOUT B1+	IO_L5P_T0U_N8_AD14P_66	9026_SCLK	IO_L18P_T2U_N10_AD2P_67
9026_SYNCOUT B1-	IO_L5N_T0U_N9_AD14 N_66	9026_RSTB	IO_L23P_T3U_N8_66
9026_SYNCOUT	IO_L4P_T0U_N6_DBC_	9026_RX1_ENABLE	IO_L23N_T3U_N9_67
B2+	AD7P_66		
9026_SYNCOUT	IO_L4N_T0U_N7_DBC_ AD7N_66	9026_RX2_ENABLE	IO_L2N_T0L_N3_67

B2-			
9026_RX1_ORX _CTRL	IO_L22P_T3U_N6_DBC_ AD0P_67	9026_RX3_ENABLE	IO_L10P_T1U_N6_QBC_AD4P_67
9026_RX2_ORX _CTRL	IO_L24N_T3U_N11_67	9026_RX4_ENABLE	IO_L18N_T2U_N11_AD2N_66
9026_RX3_ORX _CTRL	IO_L10N_T1U_N7_QBC _AD4N_67	9026_TX1_ENABLE	IO_L19N_T3L_N1_DBC_AD9N_67
9026_RX4_ORX _CTRL	IO_L18P_T2U_N10_AD2 P_66	9026_TX2_ENABLE	IO_L20N_T3L_N3_AD1N_67
9026_INT1	IO_L16P_T2U_N6_QBC_ AD3P_67	9026_TX3_ENABLE	IO_L8N_T1L_N3_AD5N_67
9026_INT2	IO_L22P_T3U_N6_DBC_ AD0P_66	9026_TX4_ENABLE	IO_L17P_T2U_N8_AD10P_66
9026_DEV_CLK _IN+	9528_9026_DEV_CLK_I N+	9026_SYSREF_IN+	9528_9026_SYSREF_IN+
9026_DEV_CLK _IN-	9528_9026_DEV_CLK_I N-	9026_SYSREF_IN-	9528_9026_SYSREF_IN-