# Octal Channel Embedded Software Radio Platform Product Brochure

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# 1 Product introduction

The eight-channel embedded software radio platform is an embedded, miniaturized, multi-channel software radio platform developed for various wireless communication product development and communication teaching. The platform is composed of two parts, one is a wireless radio frequency signal transceiver module developed based on ADI's ADRV9009 chip, and the other is a back-end digital processing module based on Xilinx's Zynq7100 chip. This platform is a high-performance, highly integrated wireless radio frequency signal transceiver processing equipment, suitable for the development of wireless communication teaching aids, miniaturized spectrum

Detection, broadband signal generator, wireless point finding and positioning development, etc. The basic performance indicators of the platform are as follows:

- Baseband processor: ZYNQ7100 integrated dual ARM Cortex™-A9 processors
- Interface: network port, optical port, serial port, USB, TF card, PL port I/O port, JTAG
- Onboard PS DDR3 1GB, PL DDR3 1GB
- Onboard 64MB QSPI FLASH
- SD card slot: can run linux operating system
- Flash and SD card switching: start from flash or from sd card start
- RF channel: 8 send 8 receive
- Sending power: maximum 0dBm
- RF working range: 75MHZ to 6GHZ
- Bandwidth: 200MHz
- Sampling rate: up to 245.76MSPS
- Volume: 23mm (length) × 15mm (width) × 15mm (height)

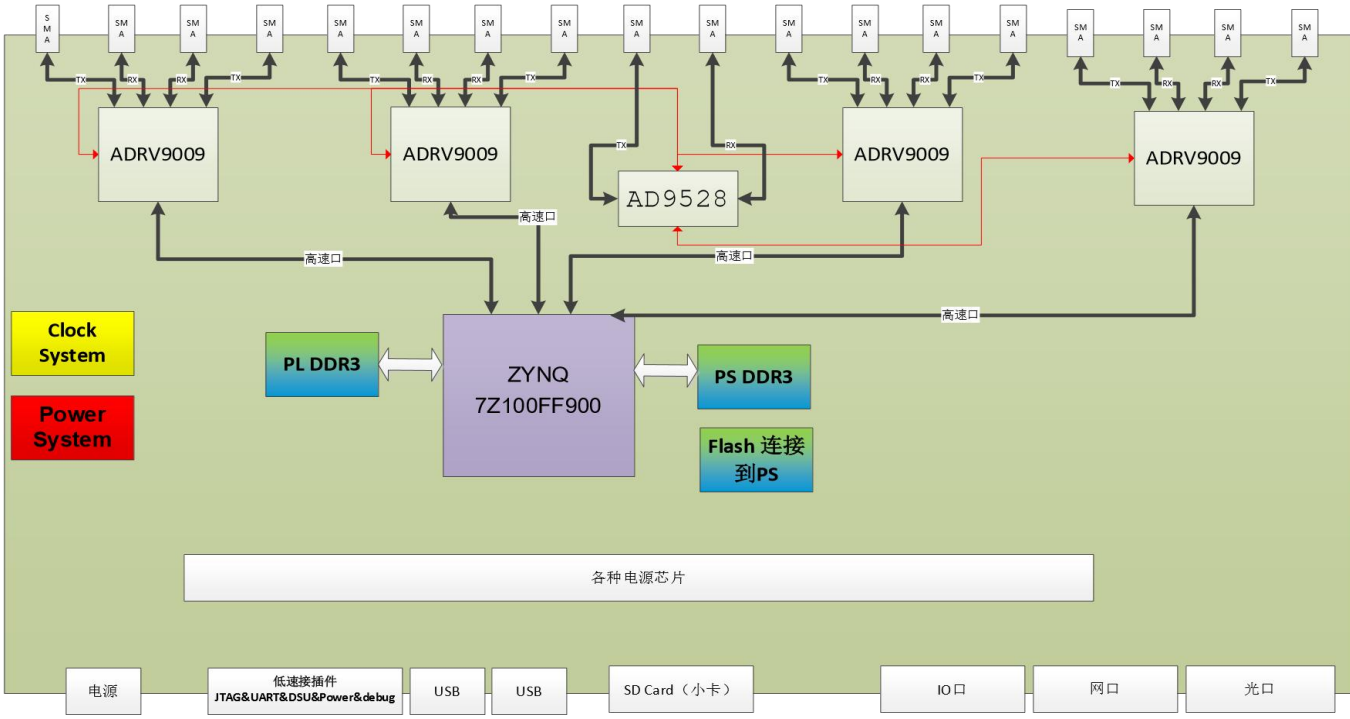



Figure 1-1 Schematic diagram of the board

## 1.1 XC7Z100-2FFG900I

The board uses the Zynq7000 series chip of Xilinx Company, the model is XC7Z100-2FFG900I. The chip's PS system integrates two ARM Cortex™-A9 processors, AMBA® interconnect, internal memory, external memory interface and peripherals. These peripherals mainly include USB bus interface, Ethernet interface, SD/SDIO interface, I2C bus interface, CAN bus interface, UART interface, GPIO and so on. PS can run independently and start on power-up or reset.

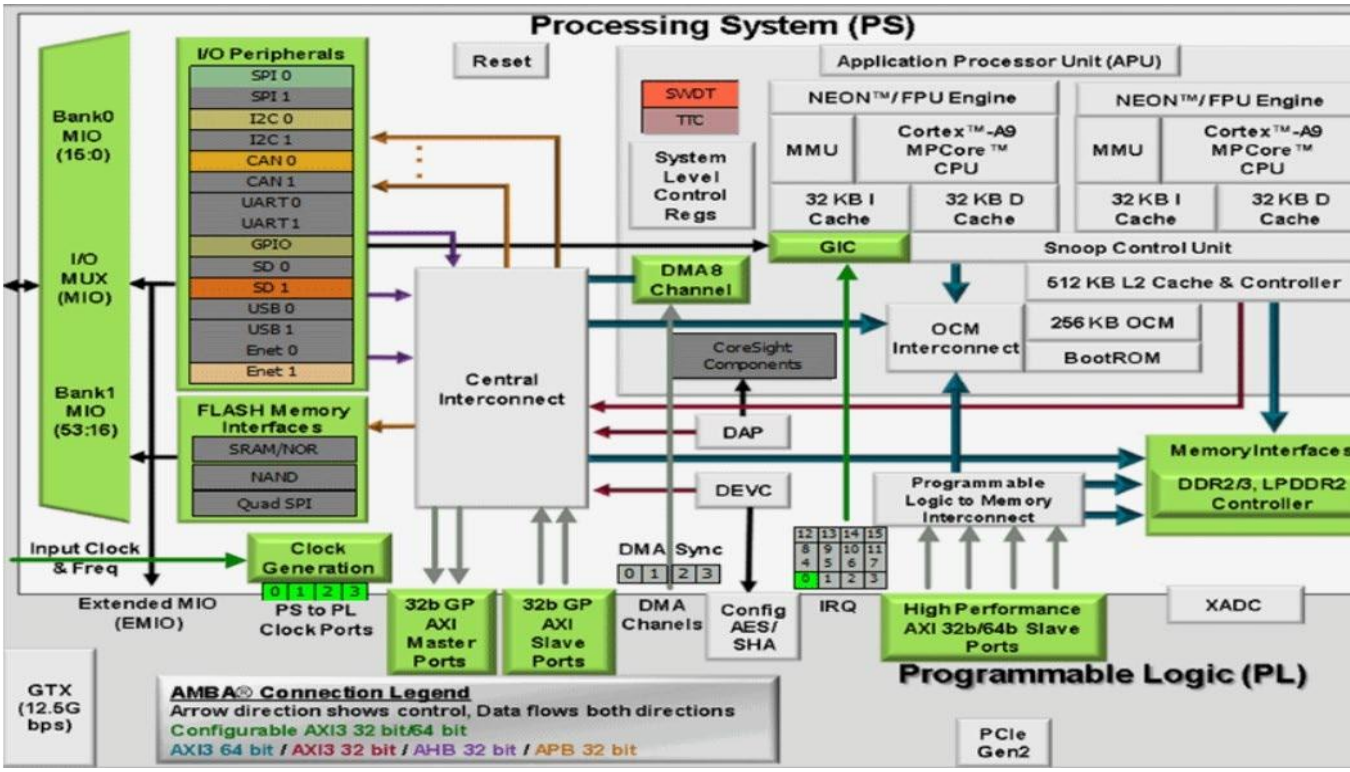



Figure 1-2 Overall block diagram of ZYNQ7100 chip

## 1.2 ADRV9009 chip introduction

ADRV9009 is a high-performance, highly-integrated radio frequency for 5G base station and radar applications

(RF)Agile Transceiver ™ Agile Transceiver . The programmability and wideband capabilities of this device make it ideal for a variety of transceiver applications. The device combines an RF front-end with a flexible mixed-signal baseband section, an integrated frequency synthesizer, and a configurable digital interface to the processor to simplify design-in.

- Has dual receivers;
- Dual input shared observation receiver;
- Maximum receiver bandwidth: 200 MHz ;
- Maximum tunable transmitter synthesis bandwidth: 450 MHz ;
- Maximum observation receiver bandwidth: 450 MHz ;
- JESD204B datapath interface;

- Tuning range: 75 MHz to 6000 MHz

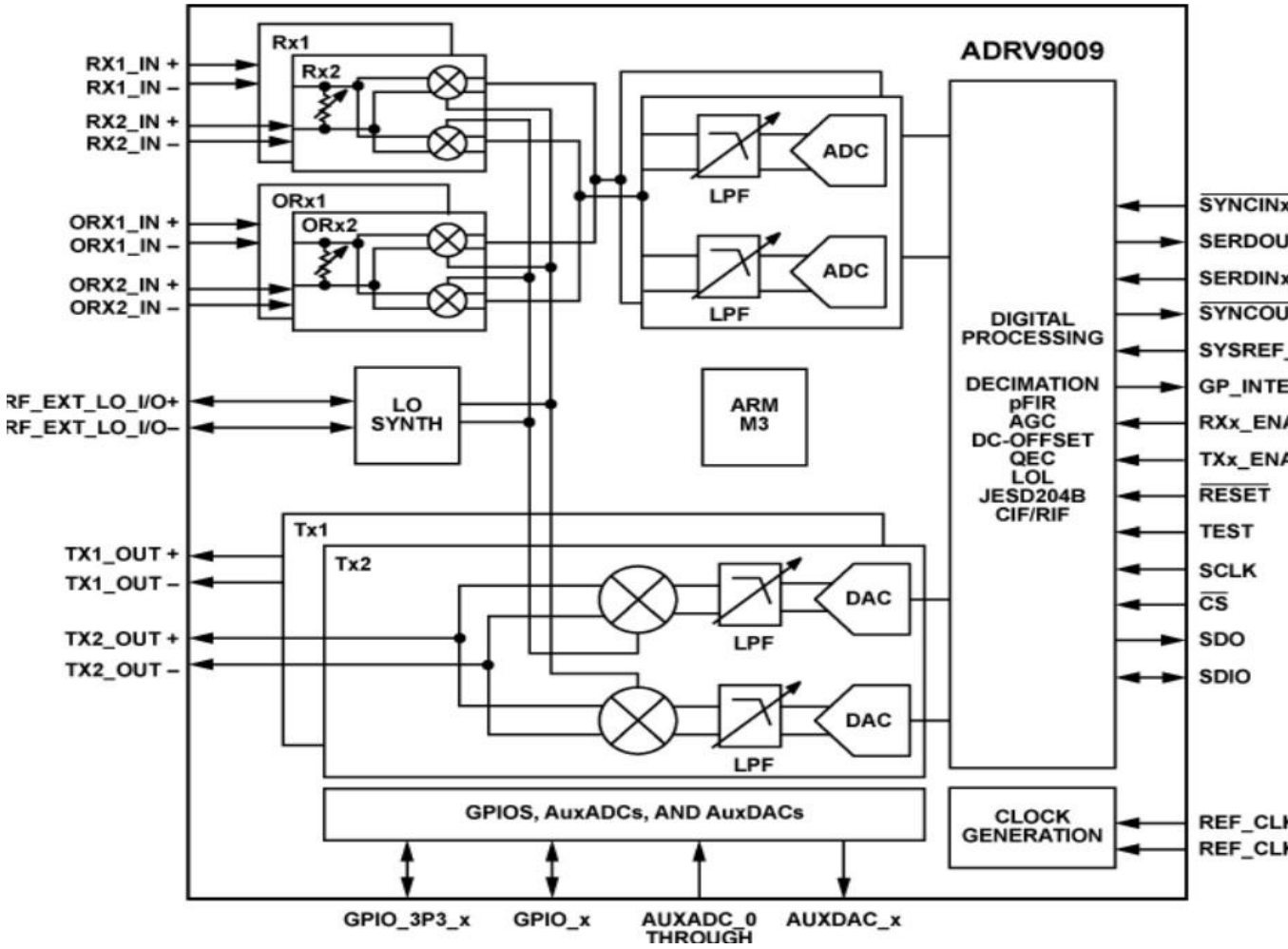



Figure 1-3 ADRV9009 principle block

## 1.3 Product in kind

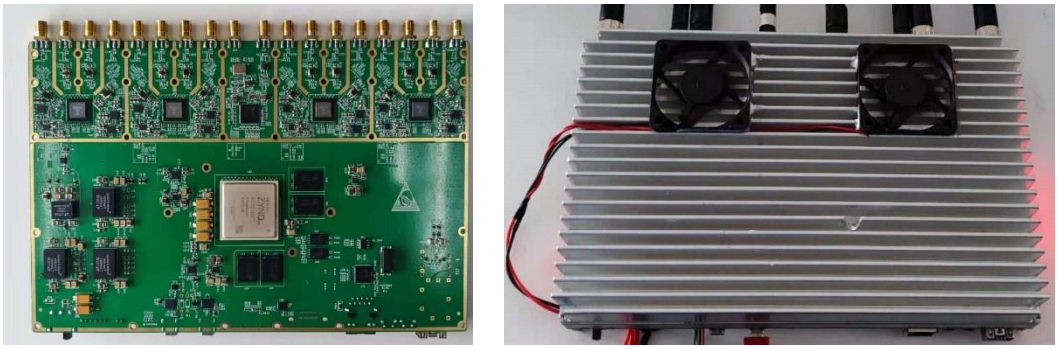


Figure 1-4 The front of the board (the picture on the right shows the effect after packing)

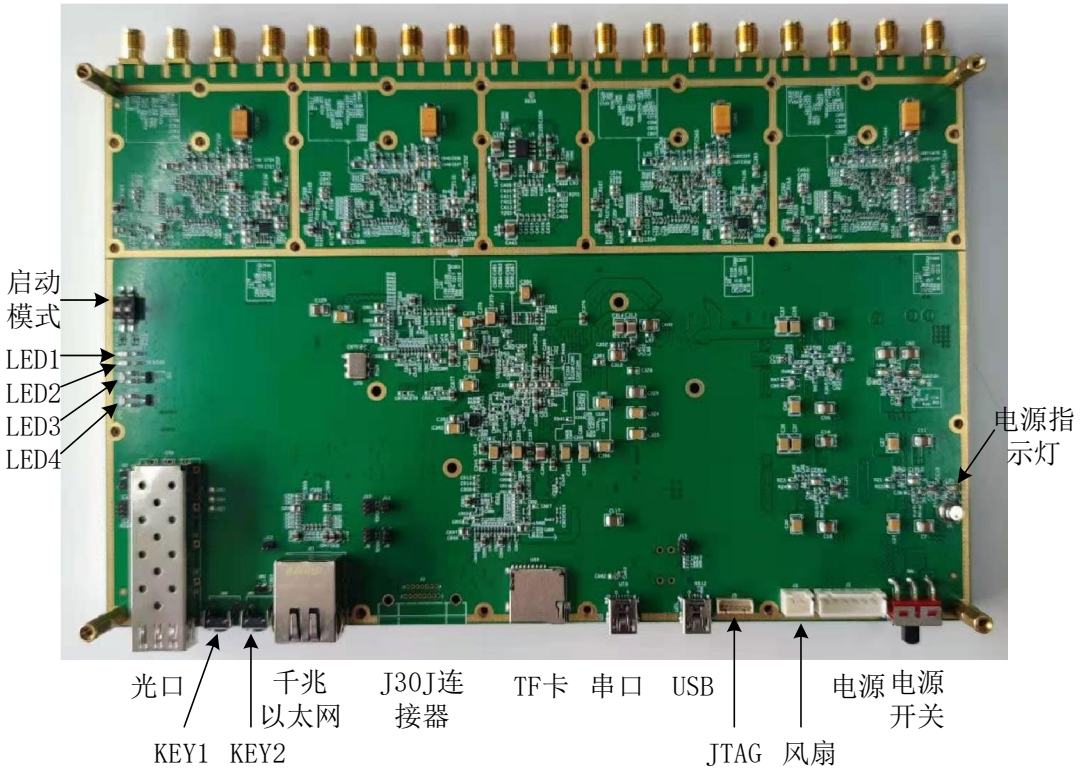



Figure 1-5 The back of the board and the definition of the interface

# 2 Interface Description

## 2.1 main power interface

The main power supply adopts +12V power supply, the maximum allowable input voltage is 14V , and the theoretical peak power consumption of the board can reach 80W . It is recommended to use a 12V10A power supply for power supply. The main power interface type is 6-pin XH2.54 interface.

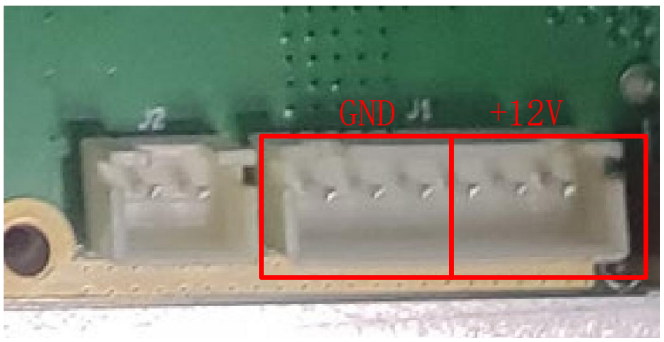



图 2-1 主电源接口

## 2.2 Fan interface

board outputs a 5.5V power supply, which can supply power for the fan. When the board is used, please install a fan for good dissipation hot, otherwise there is a risk of burnout.

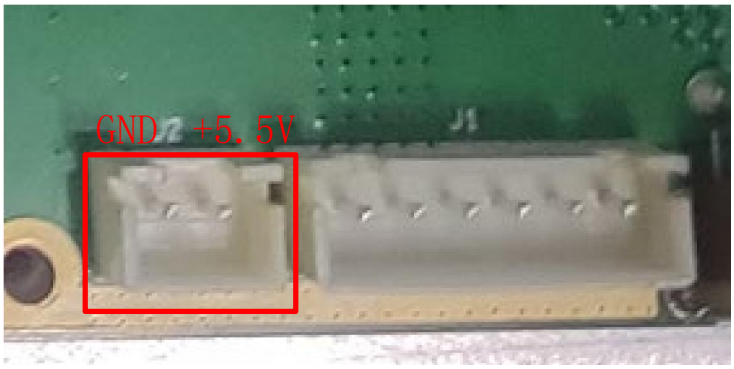



Figure 2-2 +5.5V power output

## 2.3 clock

### 2.3.1 PL clock

Onboard The 200MHz clock chip provides the clock for the PL terminal , the clock signal is a differential clock, and the level is standard LVDS .

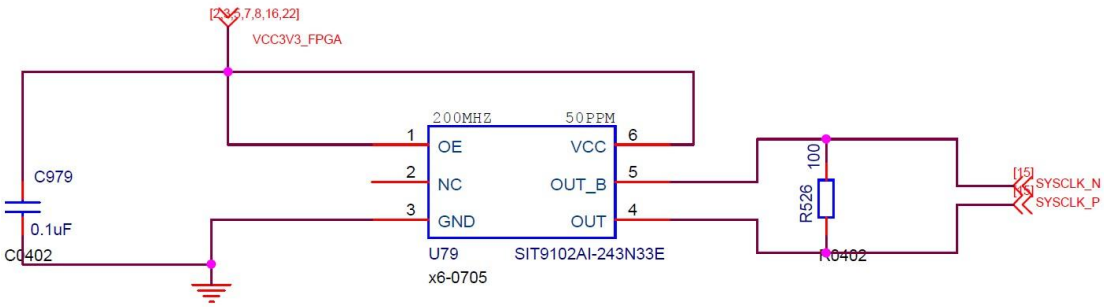



Figure 2-3 PL clock table 2-1 PL clock pin

| name | pin number | level |
|---|---|---|
| SYSCLK_P | F9 | LVDS |
| SYSCLK_N | E8 | LVDS |

### 2.3.2 ps clock

onboard The 33.333333MHz clock chip provides the clock for the PS side , the clock signal is a single-ended clock, and the level standard is LVCMOS33 .

Table 2-2 PS clock pins

| name | pin number | level |
|---|---|---|
| PS_CLK | A22 | LVCMOS33 |

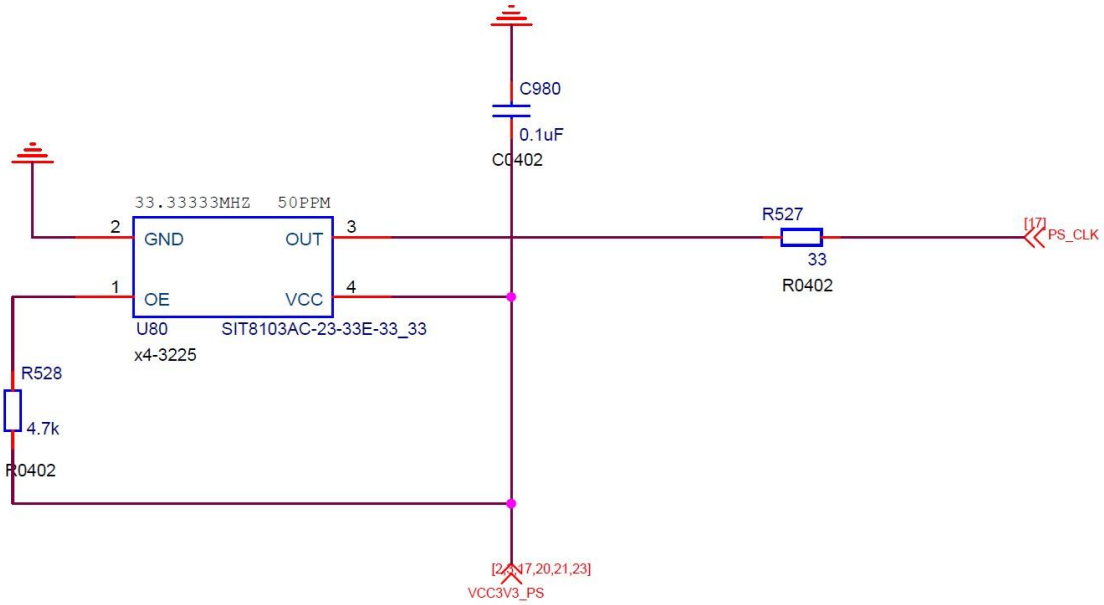



Figure 2-4 PS Clock

### 2.3.3 other

In addition to the PL clock and PS clock, there are also synchronous clocks provided by AD9528 and JESD204B data clocks on the board, which will be explained in the corresponding chapters later.

## 2.4 boot mode

The board uses a 2-bit DIP switch to switch the board boot mode, which can be selected from SD card, on-board QSPI FLASH or JTAG boot.

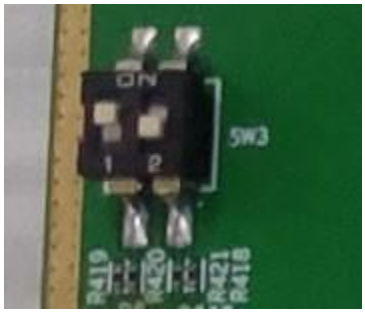



Figure 2-5 Dial the DIP switch up to 0 and down to 1.

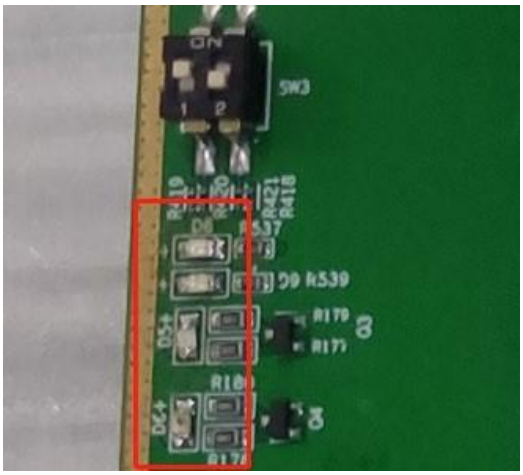
Table 2-3 Boot Mode Selection Table

| | key1 | key2 |
|---|---|---|
| SD | 1 | 1 |
| QSPI | 1 | 0 |
| JTAG | 0 | 0 |
| NAND | 0 | 1 |

## 2.5 led

There are 5 LEDs on the board , as shown in the figure below. DIP switch on the left side of the back of the board (interface side) 4 LEDs below , from top to bottom are PS side LED ( D8), PL side LED ( D9), FPGA_INIT LED (D5 ), FPGA_DONE LED ( D6). Above the main power switch on the right side of the back of the board (interface side)

There is 1 LED , which is the power indicator LED (D1 ).



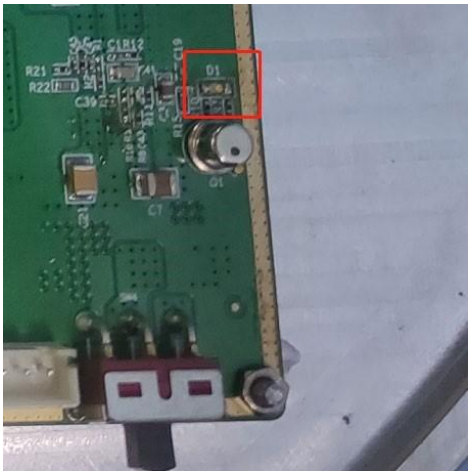
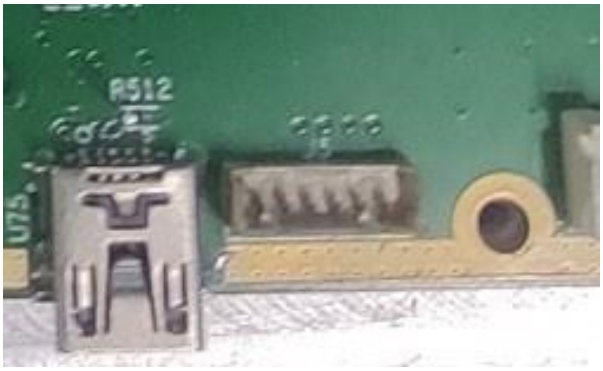



Figure 2-6 LED position table 2-4 LED pin connection table

| LED label | Connection pin name | Connection pin number | level |
|---|---|---|---|
| D8 | PS_MIO15_500 | C22 | LVCMOS33 |
| D9 | IO_L3P_T0_DQS_13 | N28 | LVCMOS25 |
| D5 | FPGA_INIT_B_0 | W9 | - |
| D6 | FPGA_DONE_0 | AA9 | - |

**2.6 JTAG** uses a 6-pin 1.25mm pitch terminal, and the silkscreen on the board is J5.




1 2 3 4 5 6

Figure 2-7 JTAG interface

Table 2-5 JTAG line sequence table

| Line order | name | Pin name | pin number |
|---|---|---|---|
| 1 | TCK-JTAG | TCK_0 | Y12 |
| 2 | TMS-JTAG | TMS_0 | V10 |
| 3 | TDO-JTAG | TDO_0 | Y10 |
| 4 | TDI-JTAG | TDI_0 | P10 |

| | | | |
|---|---|---|---|
| 5 | GND | GND | GND |
| 6 | VCC_3.3V | VCC_3.3V | Internally connected to 3.3V power supply |

## 2.7 DDR3

### 2.7.1 PS DDR3

PS side of the board is mounted with a 1GB DDR3 chip, the model is MT41K256M16-RE125, the bit width 32-bit, mounted on the BANK 502 of the 7100 chip, the BANK is a fixed BANK with DDR mounted on the PS side, and the pins are no longer listed in detail.

### 2.7.2 PL DDR3

PL side of the board is mounted with a 1GB DDR3 chip, the model is MT41K256M16-RE125, the bit width 32-bit, mounted on BANK33 and BANK34 of the 7100 chip, the detailed pin correspondence is given below, and the level standard of the specified DDR3 pin is fixed and will not be listed again.

Table 2-6 PL DDR3 pin list

| DDR3 | ZYNQ | DDR3 | ZYNQ |
|---|---|---|---|
| DDR3_DQ [ 0] | J3 | DDR3_DQS_P[0] | K3 |
| DDR3_DQ[1] | L2 | DDR3_DQS_N[0] | K2 |
| DDR3_DQ[2] | J4 | DDR3_DQS_P[1] | J1 |
| DDR3_DQ[3] | L3 | DDR3_DQS_N[1] | H1 |
| DDR3_DQ[4] | K6 | DDR3_DQS_P[2] | E6 |
| DDR3_DQ[5] | L1 | DDR3_DQS_N[2] | D5 |
| DDR3_DQ[6] | K5 | DDR3_DQS_P[3] | A5 |
| DDR3_DQ[7] | K1 | DDR3_DQS_N[3] | A4 |
| DDR3_DQ[8] | H2 | DDR3_ADDR[14] | F7 |

| | | | |
|---|---|---|---|
| DDR3_DQ[9] | G4 | DDR3_ADDR[13] | E11 |
| DDR3_DQ[10] | H3 | DDR3_ADDR[12] | L8 |
| DDR3_DQ[11] | F2 | DDR3_ADDR[11] | L10 |
| DDR3_DQ[12] | G5 | DDR3_ADDR[10] | H8 |
| DDR3_DQ[13] | H6 | DDR3_ADDR[9] | D11 |
| DDR3_DQ[14] | H4 | DDR3_ADDR[8] | G11 |
| DDR3_DQ[15] | G6 | DDR3_ADDR[7] | E7 |
| DDR3_DQ[16] | F4 | DDR3_ADDR[6] | J11 |
| DDR3_DQ[17] | D1 | DDR3_ADDR[5] | J10 |
| DDR3_DQ[18] | E5 | DDR3_ADDR[4] | H7 |
| DDR3_DQ[19] | E2 | DDR3_ADDR[3] | H12 |
| DDR3_DQ[20] | D4 | DDR3_ADDR[2] | E10 |
| DDR3_DQ[21] | E1 | DDR3_ADDR[1] | D9 |
| DDR3_DQ[22] | E3 | DDR3_ADDR[0] | D10 |
| DDR3_DQ[23] | D3 | DDR3_BA[2] | D8 |
| DDR3_DQ[24] | A2 | DDR3_BA[1] | K8 |
| DDR3_DQ[25] | A3 | DDR3_BA[0] | H11 |
| DDR3_DQ[26] | B1 | DDR3_CK_P[0] | H9 |
| DDR3_DQ[27] | B5 | DDR3_CK_N[0] | G9 |
| DDR3_DQ[28] | B2 | DDR3_RAS_N | G7 |
| DDR3_DQ[29] | C4 | DDR3_CAS_N | F8 |
| DDR3_DQ[30] | C1 | DDR3_WE_N | K10 |
| DDR3_DQ[31] | C2 | DDR3_RESET_N | D6 |
| DDR3_DM[0] | J5 | DDR3_CKE[0] | L7 |
| DDR3_DM [ 1] | G1 | DDR3_ODT [ 0] | J9 |

| | | | |
|---|---|---|---|
| DDR3_DM [ 2] | F3 | DDR3_CS_N [ 0] | K11 |
| DDR3_DM [ 3] | B4 | | |

**2.8 The FLASH** board is equipped with 64MB QSPI FLASH , which is composed of dual -channel S25FL256SAGNFI00 chips. The corresponding pins are shown in the table below.

Table 2-7 QSPI FLASH pins

| name | Corresponding pin name | Level standard |
|---|---|---|
| QSPI1_SS_B | PS_MIO0_500 | LVCOMS33 |
| QSPI0_SS_B | PS_MIO1_500 | LVCOMS33 |
| QSPI0_IO [ 0] | PS_MIO2_500 | LVCOMS33 |
| QSPI0_IO [ 1] | PS_MIO3_500 | LVCOMS33 |
| QSPI0_IO [ 2] | PS_MIO4_500 | LVCOMS33 |
| QSPI0_IO[3] | PS_MIO5_500 | LVCOMS33 |
| QSPI0_SCLK | PS_MIO6_500 | LVCOMS33 |
| QSPI1_SCLK | PS_MIO9_500 | LVCOMS33 |
| QSPI1_IO[0] | PS_MIO10_500 | LVCOMS33 |
| QSPI1_IO[1] | PS_MIO11_500 | LVCOMS33 |
| QSPI1_IO[2] | PS_MIO12_500 | LVCOMS33 |
| QSPI1_IO[3] | PS_MIO13_500 | LVCOMS33 |

## 2.9 TF card

onboard one TF card interface, its pin correspondence is as follows.

Table 2-8 TF pin correspondence

| name | Corresponding pin name | Level standard |
|---|---|---|
| SDIO_CLK | PS_MIO40_501 | LVCOMS18 |

| | | |
|---|---|---|
| SDIO_CMD | PS_MIO41_501 | LVCOMS18 |
| SDIO_DATA [0] | PS_MIO42_501 | LVCOMS18 |
| SDIO_DATA [1] | PS_MIO43_501 | LVCOMS18 |
| SDIO_DATA [2] | PS_MIO44_501 | LVCOMS18 |
| SDIO_DATA [3] | PS_MIO45_501 | LVCOMS18 |
| SDIO_CD | PS_MIO14_500 | LVCOMS33 |

## 2.10 Gigabit Ethernet interface

board has a standard RJ45 Gigabit Ethernet interface, and its PHY chip model is 88E1116R,

RJ45 port comes with a network transformer to ensure network connectivity between different network devices.

Table 2-9 Ethernet interface pin correspondence

| name | pin name | Level standard |
|---|---|---|
| ETH0-TXCLK | PS_MIO16_501 | LVCMOS18 |
| ETH0-TX0 | PS_MIO17_501 | LVCMOS18 |
| ETH0-TX1 | PS_MIO18_501 | LVCMOS18 |
| ETH0-TX2 | PS_MIO19_501 | LVCMOS18 |
| ETH0-TX3 | PS_MIO20_501 | LVCMOS18 |
| ETH0-TXCTL | PS_MIO21_501 | LVCMOS18 |
| ETH0-RXCLK | PS_MIO22_501 | LVCMOS18 |
| ETH0-RX0 | PS_MIO23_501 | LVCMOS18 |
| ETH0-RX1 | PS_MIO24_501 | LVCMOS18 |
| ETH0-RX2 | PS_MIO25_501 | LVCMOS18 |
| ETH0-RX3 | PS_MIO26_501 | LVCMOS18 |
| ETH0-RXCTL | PS_MIO27_501 | LVCMOS18 |

| | | |
|---|---|---|
| ETH0-MDC | PS_MIO52_501 | LVCMOS18 |
| ETH0-MEDIUM | PS_MIO53_501 | LVCMOS18 |

## 2.11 USB

board has a USB2.0 interface, the physical interface type is USB mini interface, and the USB interface chip is TUSB1210 . When TUSB1210 works in different modes, its REFCLK pin needs to be connected to ground or an external 26MHz reference clock, and the board is switched through a 1.27mm three-pin pin and a 1.27mm jumper cap . For specific application modes, please refer to the TUSB1210 manual and ZYNQ official manual.

Table 2-10 Correspondence to USB pins

| name | pin name | Level standard |
|---|---|---|
| USB_DATA[4] | PS_MIO28_501 | LVCMOS18 |
| USB_DIR | PS_MIO29_501 | LVCMOS18 |
| USB_STP | PS_MIO30_501 | LVCMOS18 |
| USB_NXT | PS_MIO31_501 | LVCMOS18 |
| USB_DATA[0] | PS_MIO32_501 | LVCMOS18 |
| USB_DATA[1] | PS_MIO33_501 | LVCMOS18 |
| USB_DATA[2] | PS_MIO34_501 | LVCMOS18 |
| USB_DATA[3] | PS_MIO35_501 | LVCMOS18 |
| USB_CLK | PS_MIO36_501 | LVCMOS18 |
| USB_DATA[5] | PS_MIO37_501 | LVCMOS18 |
| USB_DATA[6] | PS_MIO38_501 | LVCMOS18 |
| USB_DATA[7] | PS_MIO39_501 | LVCMOS18 |
| USB_RESET | PS_MIO47_501 | LVCMOS18 |

## 2.12 serial port

The board has a serial port and is converted into a USB interface in the board, and the physical interface type is USB mini interface, which can be directly connected to a computer through an adapter cable. The serial port conversion chip model used by the board is CP2103GM, please install the corresponding driver on the computer, otherwise the serial port will not be recognized.

Table 2-11 Corresponding serial port pins

| name | pin name | Level standard |
|---|---|---|
| UART_TX | PS_MIO48_501 | LVCMOS18 |
| UART_RX | PS_MIO49_501 | LVCMOS18 |

**2.13 The J30J connector** board has a J30J-15TJW-J connector, whose pins are connected to the PL BANK12 pins. The BANK is a 2.5V voltage supply bank, and the pins connected to the connector can be customized by the user to support any The 2.5V voltage level standard, and there are 4 pairs of pins that can be used as LVDS pairs: 2/9, 3/10, 6/4, 13/12.

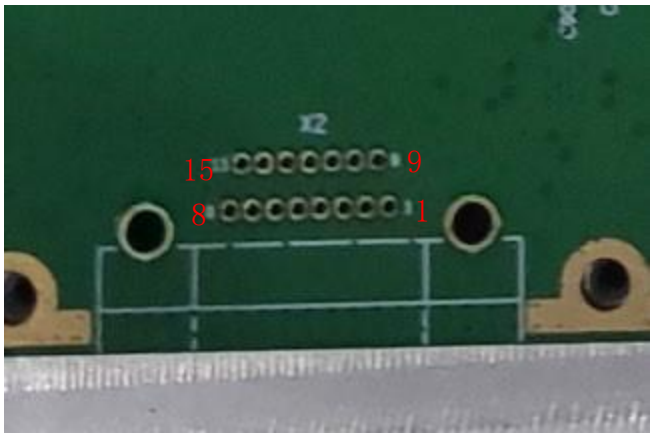



Figure 2-8 J30J-15TJW-J connector pin diagram 2-12 J30J-15TJW-J connector pin correspondence

| pin | pin name | pin number | level |
|---|---|---|---|

| | | | |
|---|---|---|---|
| 1 | IO_L22N_T3_12 | AK28 | 2.5V level |
| 2 | IO_L21P_T3_DQS_12 | AJ28 | 2.5V level |
| 3 | IO_L19P_T3_12 | AH28 | 2.5V level |
| 4 | IO_L15N_T2_DQS_12 | AG29 | 2.5V level |
| 5 | IO_L14N_T2_SRCC_12 | AF27 | 2.5V level |
| 6 | IO_L15P_T2_DQS_12 | AF29 | 2.5V level |
| 7 | IO_L13N_T2_MRCC_12 | AF28 | 2.5V level |
| 8 | IO_L8N_T1_12 | AE30 | 2.5V level |
| 9 | dangling | dangling | dangling |
| 10 | IO_L21N_T3_DQS_12 | AJ29 | 2.5V level |
| 11 | IO_L19P_T3_VREF_12 | AH29 | 2.5V level |
| 12 | IO_L16N_T2_12 | AG30 | 2.5V level |
| 13 | IO_L16P_T2_12 | AF30 | 2.5V level |
| 14 | dangling | dangling | dangling |
| 15 | dangling | dangling | dangling |

## 2.14 Button

There are two buttons on the board, the labels are SW2 and SW6 respectively, SW2 is the PS reset pin, SW6 is connected to PL IO, it is low level when pressed, which can be used as a general button.

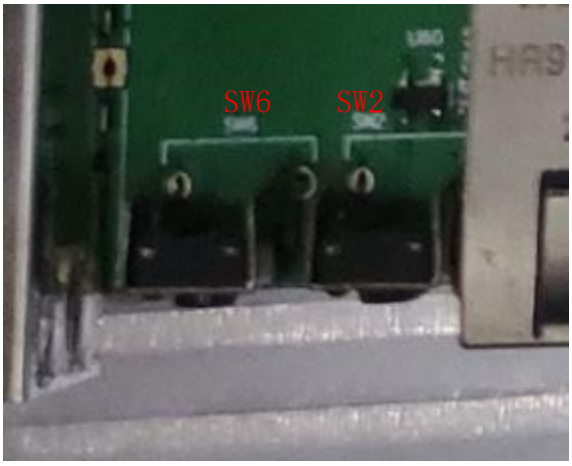



Figure 2-9 Board buttons

Table 2-13 Board button pin correspondence

| name | pin name | pin number | Level standard |
|---|---|---|---|
| SW2 | PS_POR_B_500 | D21 | LVCMOS33 |
| SW6 | IO_L7N_T1_11 | AD24 | LVCMOS25 |

## 2.15 Optical port ( SFP interface)

onboard one SFP interface, the high-speed interface of the optical port is connected to the GTX channel 0 of the 7100 BANK112 , and the clock channel 1 on the bank is used as the reference clock, and this clock channel is connected to a

156.25MHz crystal oscillator.

Table 2-14 SFP interface pin correspondence

| name | pin name | pin number | Level standard |
|---|---|---|---|
| SFP_TX_P | MGTXXP0_112 | T2 | - |
| SFP_TX_N | MGTXTXN0_112 | T1 | - |
| SFP_RX_P | MGTXRXP0_112 | V6 | - |
| SFP_RX_N | MGTXRXN0_112 | V5 | - |
| REFCLK_P | MGTREFCLK1P_112 | R8 | - |
| REFCLK_N | MGTREFCLK1N_112 | R7 | - |
| SFP_SDA | PS_MIO51_501 | F19 | LVCMOS18 |

| | | | |
|---|---|---|---|
| SFP_SCL | PS_MIO50_501 | A19 | LVCMOS18 |
| SFP_TX_DISABLE | IO_L6P_T0_9 | Y20 | LVCMOS33 |

Note: The GTX channel used by this optical port is shared with the GTX channel used by the fourth 9009 , and is switched by 4 capacitors . The 4 capacitors are connected to labels C981 , C983 , C985 , and C987 , that is, when the upper two pads among the three pads are connected, the GTX interface is connected to the optical port. The 4 capacitors are connected to labels C982 ,

C984 , C986 , C988 , that is, the lower two pads among the three pads, the GTX interface is connected to the fourth 9009 .

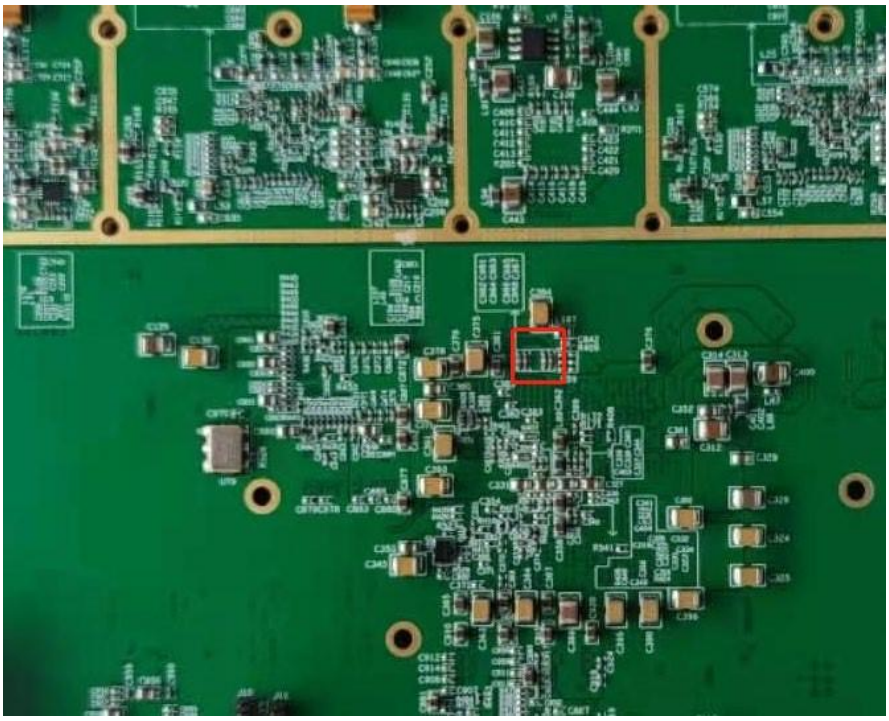


Figure 2-10 Switch capacitor position

## 2.16 AD9528

Onboard one AD9528 is used for clock synchronization of multiple 9009 chips.

### 2.16.1 clock input

The AD9528 clock is onboard 122.88MHz clock crystal, connected to the AD9528 through a matching network

11, 12 feet.

### 2.16.2 control signal

FPGA completes through SPI interface and other IO ports AD9528 control.

Table 2-15 AD9528 control signals

| name | AD9528 pin number | 7100 pin number | Level standard |
|---|---|---|---|
| REF_SEL | 4 | AD18 | LVCMOS33 |
| RESET_9528 | 19 | AD19 | LVCMOS33 |
| SPI_CS_9528 | twenty one | AA18 | LVCMOS33 |
| SPI_CLK_9528 | twenty two | AA19 | LVCMOS33 |
| SPI_DIN_9528 | twenty three | AB19 | LVCMOS33 |
| SPI_SDO_9528 | twenty four | AB20 | LVCMOS33 |
| STSREF_REQ1 | 57 | AD20 | LVCMOS33 |

### 2.16.3 clock output

AD9528 has a total of 14 clock outputs.

Table 2-16 AD9528 clock output

| name | AD9528 pin number | connect to | corresponding pin number | Level standard |
|---|---|---|---|---|
| OUT0+ | 67 | 3rd slice 9009 SYSREF_IN + | K3 | |
| OUT0- | 68 | 3rd slice 9009 SYSREF_IN- | K4 | |
| OUT1+ | 64 | 3rd slice 9009 REF_CLK_IN + | E7 | |
| OUT1- | 65 | 3rd slice 9009 REF_CLK_IN- | E8 | |
| OUT2+ | 61 | 4th slice 9009 REF_CLK_IN + | E7 | |
| OUT2- | 62 | 4th slice 9009 REF_CLK_IN- | E8 | |

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|---|---|---|---|---|
| OUT3+ | 58 | 4th slice 9009 SYSREF_IN + | K3 | |
| OUT3- | 59 | 4th slice 9009 SYSREF_IN- | K4 | |
| OUT4+ | 52 | 7100 BANK112 204B Clock + | N8 | |
| OUT4- | 53 | 7100 BANK112 204B Clock- | N7 | |
| OUT5+ | 49 | 7100 BANK111 204B Clock + | U8 | |
| OUT5- | 50 | 7100 BANK111 204B Clock- | U7 | |
| OUT6+ | 46 | 7100 BANK110 204B Clock + | AA8 | |
| OUT6- | 47 | 7100 BANK110 204B Clock- | AA7 | |
| OUT7+ | 43 | 7100 BANK109 204B Clock + | AD10 | |
| OUT7- | 44 | 7100 BANK109 204B clock- | AD9 | |
| OUT8+ | 40 | 7100 SYSREF+ | AF15 | |
| OUT8- | 41 | 7100 SYSREF- | AG15 | |
| OUT9+ | 37 | 7100 logic_122M88_P _ | AG17 | |
| OUT9- | 38 | 7100 logic_122M88_N _ | AG16 | |
| OUT10+ | 34 | 2nd slice 9009 SYSREF_IN + | K3 | |
| OUT10- | 35 | 2nd slice 9009 SYSREF_IN- | K4 | |
| OUT11+ | 31 | 1st slice 9009 SYSREF_IN + | K3 | |
| OUT11- | 32 | 1st slice 9009 SYSREF_IN- | K4 | |
| OUT12+ | 28 | The first 9009 REF_CLK_IN + | E7 | |
| OUT12- | 29 | 1st slice 9009 | E8 | |

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|---|---|---|---|---|
| | | REF_CLK_IN- | | |
| OUT13+ | 25 | 2nd slice 9009<br>REF_CLK_IN + | E7 | |
| OUT13- | 26 | 2nd slice 9009<br>REF_CLK_IN- | E8 | |